Docket No.: 0553-0401

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)
Yoshifumi Tanada	)
Application No.: 10/807,692	) Examiner: Unknown
Filed: March 24, 2004	) Group Art Unit:
For: CIRCUIT FOR INSPECTING SEMICONDUCTOR DEVICE AND INSPECTING METHOD	) Not Yet Assigned))

VERIFICATION OF TRANSLATION

P. O. Box 1450
Alexandria VA 22313-1450

Sir:

I, Reiko Sato, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, herewith declare:

that I am well acquainted with both the Japanese and English Languages; and

that to the best of my knowledge and belief the followings is a true and correct translation of the US Patent Application No. 10/807,692 filed on March 24, 2004.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 30th day of August, 2004

Reiko Sato

Name: Reiko Sato